REMARKS

Applicants respectfully request further examination and reconsideration in view of the following remarks. Claims 15-30 remain pending in the case. Claims 15-30 are rejected.

35 U.S.C. §103(a)

Claims 15-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 5,739,569 by Chen, hereinafter the "Chen" reference, in view of United States Patent 6,477,084 by Eitan, hereinafter the "Eitan" reference and/or United States Patent 5,879,990 by Dormans, et al., hereinafter the "Dormans" reference. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 15-30 are not anticipated nor rendered obvious by Eitan in view of Dormans.

Independent Claim 16 recites (emphasis added):

> A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:
>
> forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer;
>
> forming a bitline subsequent to said forming said gate comprising said polysilicon layer; and
>
> siliciding said bitline.

Claims 15 and 17-30 that depend from independent Claim 16 provide further recitations of the limitations of the present invention as claimed.

The combination of Chen, Eitan and Dormans does not teach a method for fabricating a memory cell comprising forming a gate above said channel of said substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed. Chen and the claimed embodiments of the claimed invention are very different. Applicants understand Chen to teach a non-volatile memory cell with oxide and nitride tunneling layers. As pointed out by the Examiner, Chen does not show a bitline.

With reference to Figure 2 of Chen, Applicants understand Chen to teach a memory cell having a source 10 and a drain 12. All of the source electrodes 10 are connected to a bit line (BL1 through BL4). In particular, all the drain regions 12 are connected to ground (col. 4, lines 16-18 and lines 30-32). As shown, the drain regions 12 are explicitly not connected to a bit line. Furthermore, by teaching that source electrode 10 can be connected to a bit line, and is therefore a different structure than a bit line, Chen teaches away from a source being a bit line.

Furthermore, Applicants respectfully assert that there is no motivation to combine the teachings of Chen with Eitan. Applicants understand Eitan to teach a NROM cell with a pocket implant self-aligned to at least one bit line junction. In

particular, Eitan teaches a memory cell requiring two functional bit lines for each transistor (col. 1, lines 36-40).

Applicants respectfully submit that grounding a bit line of Eitan would render Eitan inoperable for its intended purpose. In order to optimize the interconnect density in Eitan, two bit lines are used. In contrast, interconnect density is not a concern in Chen. A memory cell designer would not constrain themselves to the limitations of Eitan where there is no need for a second bit line. Therefore, there is no motivation to combine the teachings of Chen with Eitan. In contrast, by teaching a memory cell requiring two functional bit lines, Eitan teaches away from such a combination.

In view of the claim limitation of "forming a bitline subsequent to said forming said gate comprising said polysilicon layer" not being shown or suggested by the combination of Chen and Eitan, in combination with the above arguments, Applicants respectfully submit that independent Claim 16 is patentable over the combination of Chen and Eitan.

Moreover, as pointed out by the Examiner, Chen does not teach siliciding a bitline. The combination of Chen and Dormans fails to teach or suggest the claim limitation of "forming a bitline subsequent to said forming said gate comprising said polysilicon layer," because Dormans does not overcome the shortcomings of Chen. Dormans, alone or in

combination with Chen, does not show or suggest a process of fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed. As described above, Chen teaches a non-volatile memory cell with oxide and nitride tunneling layers and without a bitline.

Applicants understand Dormans to teach a semiconductor device having an embedded non-volatile memory. Dormans does not teach, show or suggest fabricating a memory cell, as claimed. In particular, Dormans does not show or suggest a process of fabricating a memory cell comprising forming a gate above said channel of the substrate, wherein the gate comprises a polysilicon layer, prior to forming a bitline, as claimed.

In view of the claim limitation of "forming a bitline subsequent to said forming said gate comprising said polysilicon layer" not being shown or suggested in Dormans, in combination with the above arguments, Applicants respectfully submit that independent Claim 16 overcome the cited references and are therefore allowable over the combination of Chen and Dormans.

Applicants respectfully assert that nowhere does the combination of Chen and Dormans teach, disclose or suggest the present invention as recited in independent Claim 16, and that this claim is thus in a condition for allowance. Therefore, Applicants

respectfully submit that the combination of Chen and Dormans also does not show or suggest the additional claimed features of the present invention as recited in Claims 15 and 17-30 which depend from independent Claim 16. Therefore, Applicants respectfully submit that Claims 15 and 17-30 overcome the Examiner's basis for rejection under 35 U.S.C. § 103(a) as these claims are dependent on an allowable base claim.

CONCLUSION

Based on the arguments presented above, Applicants respectfully assert that Claims 15-30 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

Applicants have reviewed the following references which were cited but not relied upon and do not find these reference to show or suggest the present claimed invention: U.S. 6,211,548, U.S. 6,346,442, U.S. 5,250,846, U.S. 6,518,124, U.S. 6,174,758, U.S. 2002/0142546 and JP57-177566.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge our deposit account No. 23-0085 for any unpaid fees.

Respectfully submitted,
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